REMARKS/ARGUMENTS

Claims 25-29 have been canceled.

Claim 1 has been amended and now calls for the following combination:

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity;

an epitaxially formed semiconductor layer of a second conductivity formed over said substrate;

a body region of said first conductivity formed in said epitaxially formed semiconductor layer, said epitaxially formed semiconductor layer extending below said body region ;

a source region of said second conductivity formed in said body region, said source region being adjacent an invertible channel in said body region;

a gate structure formed over said invertible channel region, said gate structure including a gate electrode which is spaced from said invertible channel by a gate insulation layer;

a drain region formed in said epitaxially formed semiconductor layer, said drain region and said body region being spaced from one another by a drift region in said epitaxially formed semiconductor layer;

a resurf region of said first conductivity formed in said epitaxially formed semiconductor layer, said resurf region being formed over at least a portion of said drift region in said epitaxially formed semiconductor layer between said body region and said drain region; and

a field plate structure disposed over said resurf region, said field plate structure including a first field plate disposed over a first insulation layer of a first thickness extending from said gate insulation layer, a second field plate disposed over a second insulation layer of a second thickness, said second insulation layer being formed over said first insulation layer, and a third field plate spaced from said second field plate by a third insulation layer of a third thickness, wherein said first field plate includes a first portion spaced from a second portion by a first gap said first portion of said first field plate extending from said gate electrode, said second field plate includes a first portion spaced from a second portion by a second gap, and said third field plate includes a first portion spaced form a second portion by a third gap, and wherein said first gap is wider than said second gap

and said third gap, and said second gap is wider than said third gap, and wherein said gaps are filled only with an insulation material; and wherein said first portion and said second portion of said second field plate, and said first portion and said second portion of said third field plate are circular and disposed around said drain region.

Fig. 15 of Fujishima does not teach or suggest a combination that includes three field plates. Fig. 19 of Fujishima does not teach or suggest a resurf region. It appears that the Examiner has taken region 20 and modified Fig. 19 to arrive at a combination which includes a resurf region and three field plates. However, no motivation has been cited that would lead a skilled person to modify the subject matter of Fig. 19 in the manner asserted. Thus, it is respectfully submitted that Fujishima does not teach the combination of a resurf region with three field plates.

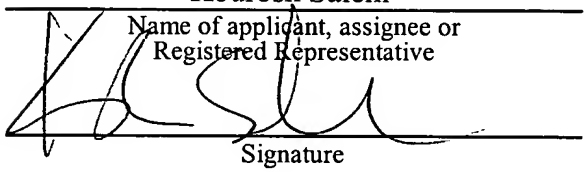
In addition, claim 1 calls for the epitaxially formed semiconductor layer to extend below the body region. Fujishima, however, only shows the Nwell 5 and Pwell 2 adjacent along a vertical wall. Nwell 5 does not extend below the Pwell 2.

Moreover, claim 1 calls for "said first portion and said second portion of said second field plate, and said first portion and said second portion of said third field plate are circular and disposed around said drain region". No reference has been shown that teaches such features, or suggests such features in combination with other limitations set forth in claim 1.

It is respectfully submitted, therefore, that claim 1 is distinguishable from the art of record. Allowance is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 18, 2007:

Kourosh Salehi
Name of applicant, assignee or Registered Representative



Signature

January 18, 2007
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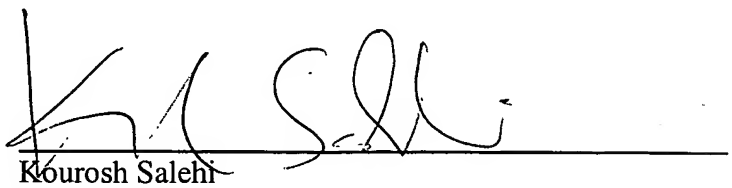
Respectfully submitted,



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